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Comparative Analysis of Array Multiplier Using Different Logic Styles

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Abstract: Multiplier is one of the most important arithmetic unit in Microprocessors and DSPs and also a major source of power dissipation. Reducing the power dissipation of multipliers is a key to satisfy the overall power budget of various digital circuits and systems. this paper elaborates the array multiplier through different logic styles. The fundamental units to design a multiplier are adders. The various types of adders used in this paper are complementary MOS (CMOS)logic style, complementary pass-transistor (CPL) logic style, double-pass transistor (DPL) logic style and domino logic style. The main objective of our work is to calculate the average power, delay and PDP of 4x4 multipliers. The design of full adder for low power is obtained and the low power units are implemented on the array multiplier and the results are analyzed for better performance. The designs are done using TANNER S-EDIT tool and are simulated using T-SPICE. The multiplier architectures are designed using the three better above said full adders and the results are compared so that we can obtain a better multiplier design.

Keywords: *Array Multipliers, Full adder, CMOS, CPL, DPL, Domino Logic power delay product***.**

I. INTRODUCTION

The core of every microprocessor, digital signal processor (DSP), and data processing application like specific integrated circuit (ASIC) is its data path. At the heart of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition. Computations needs to be performed using low- power, area-efficient circuits operating at greater speed. Addition is the most basic arithmetic operation; and adder is the most fundamental arithmetic component of the processor.

The rest of the paper is organized as follows. Section II describes the different logic styles. Section III elaborates the array multiplier. Section IV and V are followed by simulation results and conclusion.

II. LOGIC STYLES

Ila Gupta et al. has proposed a large number of CMOS logic design styles [5]. For multiplication, adder is used as a basic element. For arithmetic applications, following three different logic styles are used for a full adder design to achieve best performance results for multiplier design [6].

A. Conventional Static CMOS-CSL

The recent VLSI arithmetic applications [6] i.e 4-bit RCA, uses conventional static CMOS logic. The schematic diagram of a conventional static CMOS full adder cell is illustrated in figure 1.

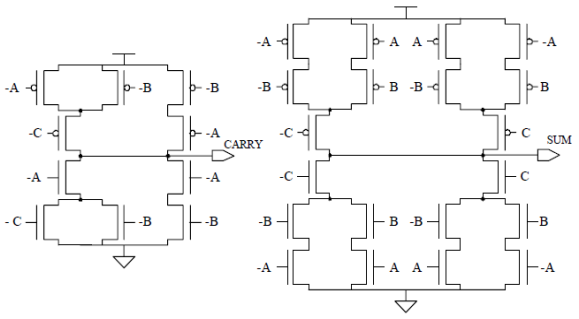

Fig 1: CSL Logic Full adder

The signals noted with '-' are the complementary signals. The p- MOSFET network of each

stage is the dual network of the n- MOSFET. Advantages of the CMOS logic style are its robustness against voltage scaling and transistor sizing (high noise margins) and thus reliable operation at low voltages and arbitrary (even minimal) transistor sizes (ratio less logic).

B. Complementary Pass Transistor Logic-CPL

The basic difference of pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation,which results in a smaller number of transistors and smaller input loads, especially when NMOS networks are used.CPL [7] uses only an n-MOSFET network for the implementation of logic functions, thus resulting in low input capacitance and high-speed operation [8]. The schematic diagram of the CPL full adder circuit is shown in figure 2. Because the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs [9].The advantages [10] of pass logic transistors include – Smaller number of transistors and smaller input loads, along with MUX and especially XOR circuits being implemented efficiently. The disadvantage [10] of pass transistor logic is that threshold voltage drops through the NMOS transistors makes it necessary to maintain output voltage level; hence inverter is used at output which increases the number of transistors.

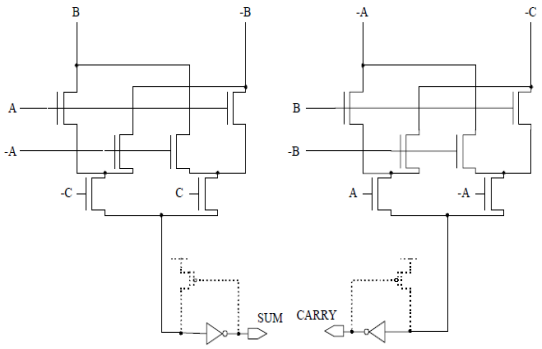

Fig 2: CPL Logic Full adder

C. Double Pass Transistor Logic-DPL

DPL [11][12] is a modified version of CPL. The circuit diagram of the DPL full adder is given in figure 3. In DPL circuit full swing operation is achieved by simply adding p- MOSFET transistors in parallel with the n-MOSFET transistors. Hence, the problems of noise margin and speed degradation at reduced supply voltages, which are caused in CPL circuits due to the reduced high voltage level, are avoided.

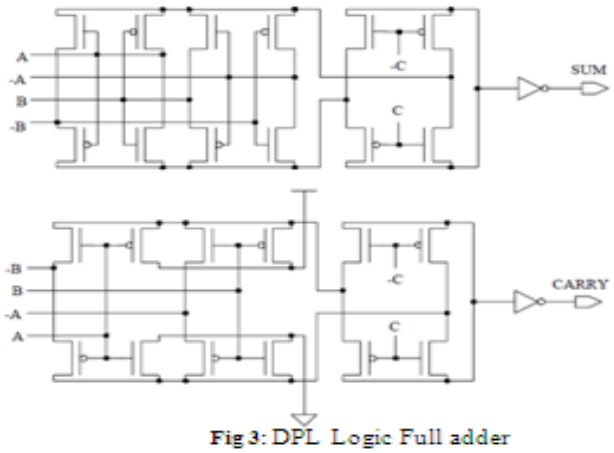

Fig 3: DPL Logic Full adder

Thebasic difference of pass-transistorlogic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads, especially when NMOS networks are used. However, the threshold voltage drop ($Vout = Vdd - Vtn$) through the NMOS transistors while passing

logic "1" makes swing (or level) restoration at the gate outputs necessary in order to avoid static currents at the subsequent output inverters or logic gates

D. Domino Logic

Domino logic circuits have many advantages such as high speed of operation, minimum used area, low noise margins, and the most important of all, they offer potential power consumption savings since the overall gate capacitance is smaller than their static counterparts [21-25]. For this reason circuit design using domino logic tends to be a very attractive method for high performance, low-power designs.

The basic structure of domino logic is shown in Fig. 4. It is a non-inverting structure, and consists of a nMOS transistor network, which implements the required logic function, two transistors (an *nMOS* and a PMOS) where the clock signal is applied and synchronizes the operation of the circuit, and a static CMOS inverter which provides the circuits output.

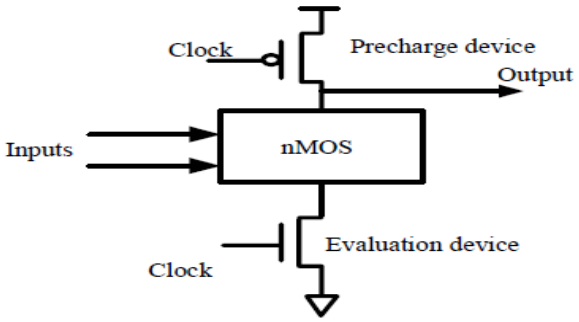

Fig.4 Basic structure of Domino Logic

The period where CLK is low is called the precharge phase. In this phase the internal node, F is charged to power supply voltage while the output node, F, is discharged to ground. The period where CLK is high is called the evaluation phase. In this phase the values of the inputs determine the discharge (F = 0) or not (F = 1) of the internal node The inverter in the output of a domino logic circuit is included for several reasons**.** First, it is required for proper operation of a chain of domino gates. Second, the internal node F is a weak node, when the clock is high, the high value on that node is not driven [8].

Fig. 5 shows the schematic of the CARRYOUT circuit. The core of this circuit is the domino logic that implements the function of CARRYOUT[9]. This circuit will stay in standby phase when the clock signal *CLK* is „logic 1 . It will turn in the evaluating phase if the clock signal *CLK* is „logic 0 . For the high-speed operation, the inverter *I*1 is designed in multi- threshold methodology where a low-*Vt* PMOS transistor is connected with a high-*Vt* NMOS transistor such that the logic 0 can pass the inverter at a higher speed.

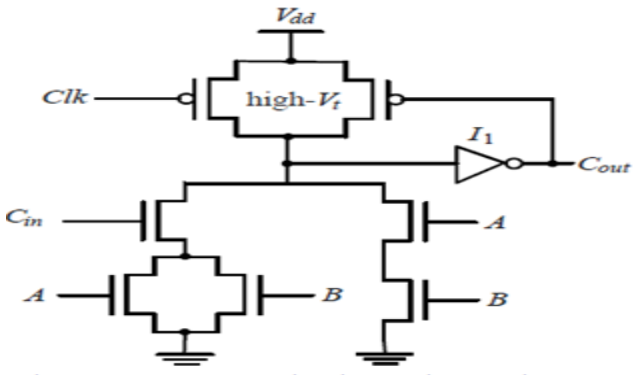

Fig.5: CARRYOUT Circuit Domino Logic AND Gate

The Circuit for SUM Operation Fig. 6 shows the schematic of the SUM circuit. The SUM circuit is composed of two XOR gates. The XOR gate is modified from the cross-coupled version by replacing the NMOS portion with a clock gated NMOS. In this circuit, the PMOS transistors receive the input signal A, B, and Cin. The operation of this circuit can be divided into two phases: the IDLE PHASE and the EVALUATING PHASE. In the IDLE PHASE, the clock signal CLK is „logic 1 , and the output signal SUM will be „logic 0 . In the EVALUATING PHASE, the clock signal CLK is

„logic 0 , and the corresponding output signal SUM will be evaluated according to the input signals A, B, and Cin.

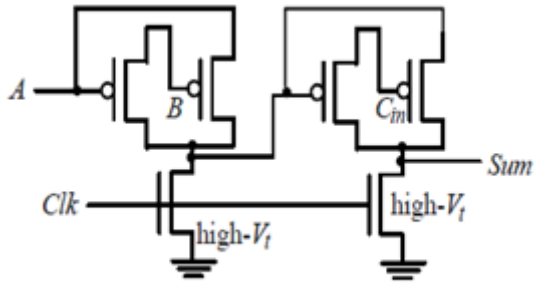

Fig 6. SUM Circuit

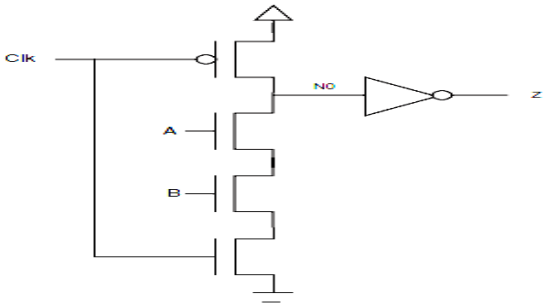

Fig.7: 2 input AND Gate using Domino Logic

III. ARRAY MULTIPLIER

An array multiplier is very regular in structure as shown in figure 4. It uses short wires that go from one full adder to adjacent full adders horizontally, vertically or diagonally [13]. An n × n array of AND gates can compute all the *i i a b* terms simultaneously. The terms are summed by an array of 'n [n - 2]' full adders and 'n' half adders. The shifting of partial products for their proper alignment is performed by simple routing and does not require any logic. The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders. Each row of full adders or 3:2 compressors adds a partial product to the partial sum, generating a new partial sum and a sequence of carries.

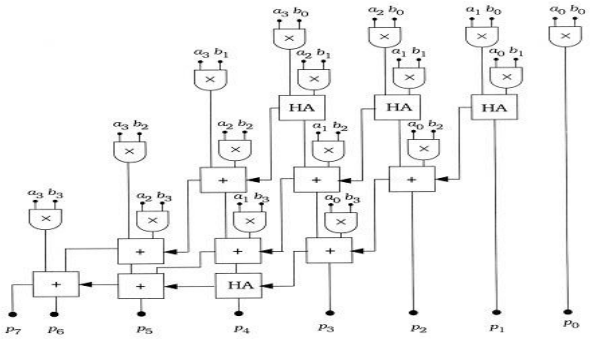

Fig 8: 4-bit Array Multiplier (AM)

The delay associated with the array multiplier is the time taken by the signals to propagate through the AND gates and adders that form the multiplication array. Delay of an array multiplier depends only upon the depth of the array not on the partial product width. The delay of the array multiplier is given by [14]:

$$(T\ critical) = [(N-1) + (N-2)]*T(Carry) + (N-1)*T(Sum) + T(AND) \quad 3)$$

ere T (*Carry*) is the propagation delay between input and output carry, T (*Sum*) is the delay between the input carry and sum bit of the full adder, T (*AND*) is the delay of AND gate, N is the length of

multiplier operand. The advantage of array multiplier is its regular structure. Thus it is easy to layout and has small size. In VLSI designs, the regular structures can be tiled over one another. This reduces the risk of mistakes and also reduces layout design time. This regular layout is widely used in VLSI math co-processors and DSP chips [15].

IV. SIMULATION RESULT

The 4-bit multipliers are compared based on the performance parameters like propagation delay, and power dissipation. To achieve better performance, the circuits are designed using CMOS process by MOSIS in 180 nm technology. All the circuits have been designed using TANNER EDA[16].

Table I Comparative analysis of Array Multiplier Using Different Logic Style Full Adder

Logic Style	Delay(ns)	Power(uw)	PDP(FJ)
CMOS	8.30	10.73	89.06
CPL	4.33	24.70	131.82
DPL	4.66	19.72	92.03
Domino	4.05	5.52	22.35

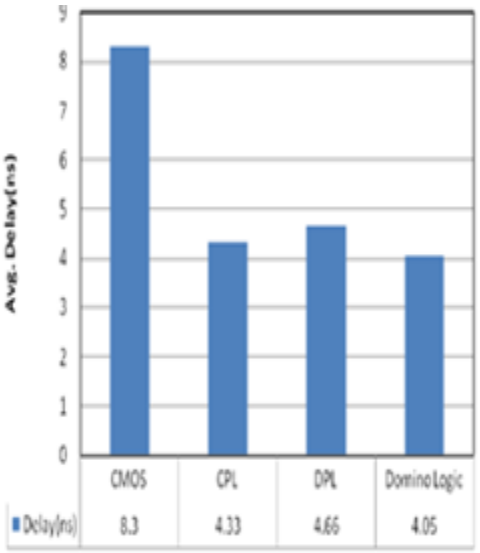

Fig 9: 4-bit Array Multiplier (AM)

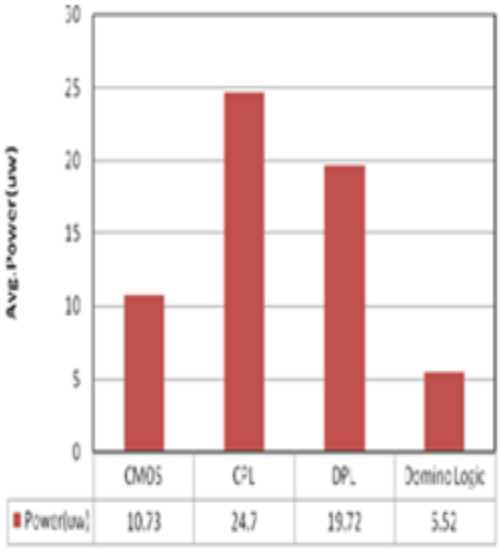

Fig 10: 4-bit Array Multiplier (AM)

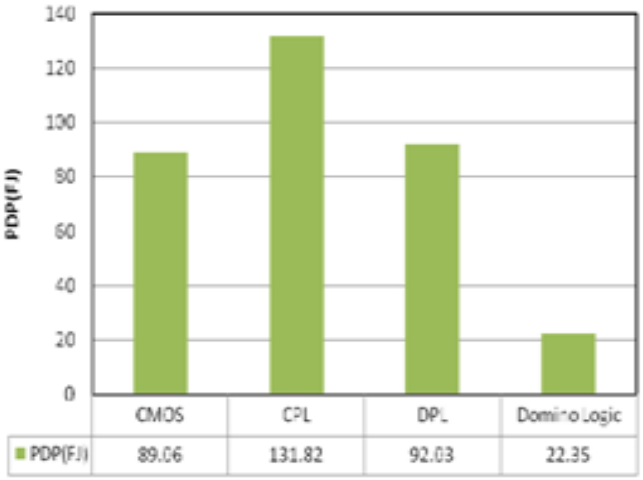

Fig 11: 4-bit Array Multiplier (AM)

Table I shows the simulation result of 4x4 array multipliers through different logic styles, similarly figure 9,figure 10 and figure 11 shows the delay power and PDP of different logic style array multiplier respectively. Figure 10 shows the minimum power dissipation for Domino logic while maximum power dissipation for CPL based array multiplier.

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V. CONCLUSION

It has been observed that Domino logic design style exhibit better characteristics (speed and power) as compared to other design styles. So, Domino logic style can be used where power and high speed is the prime aim. Where, Domino logic

consumes the lowest power among the four. so Domino logic can be considered best logic design style with respect to all parameters of 4-bit array multiplier architectures as shown in Table I.

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